

**REMARKS**

Claims 4-5, 8-10, and 13-21 are pending in this application. Claims 1-3, 6-7, and 11-12 have been canceled in order to facilitate early allowance. Applicants reserve the right to present these claims later and/or in a continuation application. Claims 4-5, 8, 10, 13, and 15 have been amended.

Claims 4, 8, and 13 have been amended to be independent of a rejected base claim and maintain the subject matter and scope as originally drafted. Claim 5 has been amended to incorporate the subject matter of claims 1 and 2. Claim 10 has been amended to incorporate the subject matter of claims 1 and 6. Claim 15 has been amended to correct a typographical error.

Applicants respectfully request that a timely Notice of Allowance be issued in this case based on the following remarks.

**I. ALLOWABLE SUBJECT MATTER**

Claims 4, 8, 9 and 13-21 are objected to as being dependent upon a rejected base claim. Claims 4, 8, and 13 have been amended to be in independent form including all of the limitations of the base claim and any intervening claims.

Therefore, it is respectfully requested that this objection of claims 4, 8, 9 and 13-21 be removed.

**II. CLAIM REJECTIONS UNDER 35 U.S.C. § 103.**

Claims 1-3, 6-7, and 10-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lane et al. paper entitled "The design of Thin-Film polysilicon resistor for analog IC applications" in view of Applicants' Admitted Prior Art.

Claims 1-3, 6-7, and 11-12 have been canceled in order to facilitate early allowance. As such, only claim 10 remains subject to this rejection.

Claim 10 has been amended to incorporate the subject matter of canceled claims 1 and 6. Additionally, claim 10 has been amended to include claim language regarding the fit parameters that the Office Action has indicated as allowable subject matter. For at least this reason, claim 10 is not taught by the cited references and withdrawal of this rejection is respectfully requested.

**III. CLAIM REJECTIONS UNDER 35 U.S.C. § 103.**

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Lane et al. paper entitled "The design of Thin-Film polysilicon resistor for analog IC applications" in view of Joy et al. paper entitled "Thermal Properties of very Fast Transistor".

Withdrawal of this rejection is respectfully requested for at least the following reasons.

Establishment of a prima facie case of obviousness requires that the references, when combined, teach or suggest all of the claim limitations. Additionally, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Claim 5 includes claim language that the thermal resistance comprises calculating the thermal resistance according to the formula:

$$r_{th} = z/\lambda(LW + 2H(L + W))$$

***Neither Lane et al. or Joy et al. teach such a formula as in claim 5.***

The Office Action states that Lane et al. do not teach thermal resistance relative to the height of the thin film resistor. The Office action relies on Joy et al. as teaching thermal resistance relative to the height of the film resistor and references a citation on page 587, col. 2, lines 5-12 as allegedly teaching thermal resistance associated with L, W, and H. However, this citation merely relates to power dissipated for a depletion region of a transistor at a depth D whereas H is approximately the *thickness of the depletion region*, not a height of a thin film resistor. Thus, the combined references fail to teach the feature of claim 5.

***Lane et al. and Joy et al. are not properly combinable***

As stated above, a combination of the cited references fails to teach the claimed invention. However, even if the art did teach the above feature, claim 5 is patentable because the combination of the cited art is improper for at least the following reasons. Lane et al. relate to the design of thin-film polysilicon resistors. In contrast, Joy et al. relate to thermal properties of very fast transistors by developing a mathematical model of three-dimensional transient heat flow. (Page 386, paragraph 1-2) Joy et al. do employ power dissipation in their discussion, but do not attempt to model resistance characteristics of thin film resistors. Thus, one of ordinary skill in the art having evaluated Joy et al. would not have been motivated to look to Lane et al. since Lane et al. do not even consider thermal issues therein.

All of the requirements to establish a prima facie case of obviousness are not met, as described above. Accordingly, withdrawal of this rejection of claim 5 is respectfully requested.

**V. CONCLUSION**

For at least the above reasons, pending claims currently under consideration are believed to be in condition for allowance and notice thereof is requested.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36776.

Respectfully submitted,  
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By



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**CERTIFICATE OF MAILING (37 CFR 1.8a)**

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: September 15, 2005

  
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